It is my great pleasure to welcome you to the main EUROMICRO event, the joint 16th Digital Systems Design (DSD 2013) and the 39th Software Engineering and Advanced Applications (SEAA 2013) Conferences. The unique integration of these two high quality conferences provides an opportunity for interdisciplinary research to be presented and enables scientists to observe connections as well as collaboration opportunities among diverse but highly interrelated fields.

I am honored to host the DSD/SEAA event in Santander, the capital of the autonomous community and historical region of Cantabria situated on the north coast of Spain. The northern regions of Spain are often less known to foreign visitors, but this area keeps some of the jewels of the country: amazing landscapes and charming beaches, a rich historical heritage, friendly peoples and natural preserves.

Santander spreads along the bay and the ocean. There are several beaches and harbors limiting the city on the northern side, towards the southern part you’ll find the old city centre and a bit further the green mountains. We could say that Santander is between the blue and the green. Santander is an important tourism destination in Spain. Besides its appeal as a holiday resort, the city is becoming an important centre for congresses and conferences. Additionally, the whole region of Cantabria has a wide range of opportunities and excursions for exploring the nature, with beautiful mountains, prehistoric sites, sky resorts, beautiful villages and world heritage sites such as the Altamira caves with prehistoric paintings, the park of Cabárceno, the charming village of Santillana del Mar, Comillas, San Vicente de la Barquera, Suances and Laredo, famous for their beaches.

This year the quantity of submissions was beyond our expectations. Program committees of SEAA and DSD have done an excellent work of reviewing and selecting the papers. I would like to first thank all the authors for their high quality research and their decision to present their work in DSD/SEAA. We would like to thank the program chairs, José Silva Matos, Francesco Leporati (DSD), Onur Demirors and Oktay Türetken (SEAA), the track chairs, the program committees and associated reviewers for selecting high quality work and providing significant feedback to the authors. They are behind the high technical quality of both conferences.

We also would like to take this opportunity to thank the organization committee members Michael G. Harbour, Ramón Beivide, Pablo Sánchez and the Fundación Leonardo Torres Quevedo, the publication chair Amund Skavhaung, the researchers of the GIM-GESE, Luis Muñoz from SmartSantander, the University of Cantabria and the City Council of Santander. All of them have actively contributed to the organization of the DSD/SEAA event.

We hope the conference in Santander will bring the relaxing atmosphere for a profitable scientific experience and a wonderful personal stay.

Eugenio Villar
Euromicro DSD/SEAA 2013 General Chair
We cordially welcome you to the 39th Euromicro Conference on Software Engineering and Advanced Applications (SEAA), September 4-6, 2013 in Santander, Spain.

The Euromicro SEAA conference series is a long-standing international forum for researchers, practitioners from business and industry, and students to present and discuss the latest innovations, trends, experiences, and concerns in the field of Software Engineering and Advanced Applications in information technology for software-intensive systems. Over the years, Euromicro SEAA series have reflected and represented the continuous changes in this area by focusing on new, innovative and advanced software engineering methodologies and applications. The 39th Euromicro SEAA continues this tradition with several tracks and special sessions that reflect up-to-date trends in research and practice.

This year’s main tracks include:

• Model-Based Development, Components and Services (MOCS)
• Software Process and Product Improvement (SPPI)
• Software Management (SM)
• Embedded Software Engineering (ESE)
• Cloud Software (CS)

In addition to these tracks, the program includes three special sessions on emerging and promising topics that are likely to have an impact in the near future:

• Estimation and Prediction in Software & Systems Engineering (EsPreSSE — inside the SM track);
• Measurement as a strategy for Software Value Management (MeSVAM — inside the SPPI track);
• Workshop Session on Teaching, Education and Training for Dependable Embedded and Cyber-physical Systems (TET-DEC).

This year, SEAA has received 121 submissions that have been rigorously peer reviewed by the program committee members and reviewers. As a result, 45 were accepted as full papers and 16 as short papers. We believe that these accepted contributions constitute a stimulating program and will provide many new ideas and insights.
Many people have contributed to make this year’s event possible and successful. First, we are grateful to the General Chair Eugenio Villar for his coordination and support. We would like to thank the chairs of all the tracks and special sessions:

- Kung-Kiu Lau and Tomas Bures for organizing the MOCS track,
- Stefan Biffl and Rick Rabiser for organizing the SPPI track,
- Alain Abran and Michel Chaudron for organizing the SM track,
- Jan Carlson, Patrick Graydon, and Mark Bartlett for organizing the ESE track,
- Ivan Porres for organizing the CS track,
- Rudolf Ramler and Dietmar Winkler for organizing the EsPreSSE special session,
- Cigdem Gencel and Maya Daneva for organizing the MeSVAM special session, and
- Erwin Schoitsch and Amund Skavhaug for organizing the TET-DEC workshop-session.

We would also like to thank Erwin Grosspietsch and Konrad Klöckner in organizing the Work-In-Progress session for novel ideas in the field.

Special thanks go to the organizing team; Brigitte Klöckner from the Euromicro office, the proceedings chair Amund Skavhaug, publicity chair Erdir Ungan, and Webmaster Serap Yagmur.

Finally, we thank all the authors, presenters, and participants of this year’s conference.

Onur Demirors and Oktay Turetken
Euromicro SEAA 2013 Program Chairs
“Computing Platforms for the XXI Century”

Abstract

Wikipedia define Platform as “A raised level surface on which people or things can stand”. A more familiar technical interpretation applies to the hardware and OS configuration applicable to the execution of software; most frequently applicable to highly stable PC or Mainframe architectures.

But the world has changed a lot since serious computing power moved into the embedded consumer arena. Now, with runs of many millions for single products, the argument for customisation is much more justifiable; so the traditional view of platforms is struggling against a tide of individuality.

Can the ARM architecture bring stability back into this chaos, or is something else needed?

Isaac Newton realised the reality of platforms when he talked of standing on the shoulders of giants. A platform is a stable place where engineers and scientists can stand to achieve more than they would otherwise have done. So our XXI Century Platforms are the shape to deliver improved Productivity, Reuse, Quality, TTM, Cost, etc. for the System Products we are now charged to deliver. Its business, stupid!
Antonio Gonzalez
Director, Intel Labs Barcelona

“Resilient Architectures for Energy-Efficiency”

Abstract

Moore’s law will continue to provide us with the capability to integrate more devices in the same area, but the benefit of this ever increasing computing density is jeopardized by the difficulties to dissipate the increased power it requires. On the other hand, smaller devices will be more susceptible to faults and will exhibit an increasing degree of variability in their behavior. In this scenario, innovative solutions to reduce power and maintaining a high-degree of reliability through more resilient architectures are going to be key to harness the benefits of Moore’s law in order to keep delivering an increased performance to the end user. In this talk I will outline some research avenues based on this approach.
Mehmet Aksit (Akşit)

Professor at the Department of Computer Science, University of Twente.

“Gummy Modules for Coping with Emergent Behaviour”

Abstract

The term emergence in software is defined as the appearance of complex behaviour out of multiplicity of relatively simple interactions. In the design of navigation systems, weather forecasting systems, pollution monitoring systems, stock market management systems, for example, software engineers typically deal with certain kind of emergent behaviour. Software systems that deal with emergent behaviour are in general complex, exhibit dynamic behaviour, and are typically designed to be long-lived. These characteristics demand proper modularization of such software systems. Unfortunately, current module-based, object-oriented and aspect-oriented languages lack language abstractions to represent emergent behaviour satisfactorily. In this talk, with the help of some real world examples, emergent behaviour will be defined. Second, current languages and their shortcomings will be illustrated. To overcome their limitations, new language abstractions, called gummy Modules will be introduced. Gummy Modules assume events (state-changes) as the bases for modularization. They are more expressive than current aspect-oriented languages because they explicitly abstract and encapsulate appearance and disappearance of emergent behaviour. Finally, this talk will end with some example applications of Gummy Modules.
Rory O’Connor
Senior Lecturer in the School of Computing

“Inside International Standards: A Contributor’s Perspective”

Abstract

International standards such as those supported by organizations like the ISO generally have a poor reputation with certain sections of academia and industry. Whilst there may be many publicised business advantages of using standards, standardization is an often-neglected route for exploiting academic and commercial research. Often researchers have little or no experience of standardization to plan, implement and exploit their research utilizing standards, and therefore trying to achieve the maximum potential from their research endeavours. Involvement of standards development organisations in your research ensures international recognition, since clearly the international community regards the work sufficiently highly to invest in writing standards based upon your research. Recognition in this way has the potential to highlight in a world stage your research and enhance your international reputation.

As part of this keynote address, I will examine issues such as: the benefits of standards for industry and academia, the benefits of being directly involved in the standards community for both industry and academia and specifically how standards can inform your research. Based upon personal experience as Ireland head of delegation to the ISO (ISO/IEC JC1/SC7) and that of editor of ISO/IEC 29110-2, I will examine the issues and benefits of becoming actively involved inside the standardization community and how this can be translated into research.
Abstract

Microfluidic biochips integrate different biochemical analysis functionalities (e.g., dispensers, filters, mixers, separators, detectors) on-chip, miniaturizing the macroscopic chemical and biological processes often processed by lab-robots, to a sub-millimeter scale. These microsystems offer several advantages over the conventional biochemical analyzers, e.g., reduced sample and reagent volumes, speeded up biochemical reactions, ultra-sensitive detection and higher system throughput, with several assays being integrated on the same chip. Hence, microfluidic biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the necessary functions for biochemical analysis. Microfluidic biochips have an immense potential in multiple application areas, such as clinical diagnostics, advanced sequencing, drug discovery, and environmental monitoring, to name a few. Consequently, over the last decade, biochips have received significant attention both in academia and industry. The International Technology Roadmap for Semiconductors 2011 has listed “Medical” as a “Market Driver” for the future, and many companies related to biochips have already emerged in recent years and have reported significant profits.

There are several types of microfluidic biochips, each having advantages and limitations. In flow-based biochips the microfluidic channel circuitry on the chip is equipped with chip-integrated micro-valves that are used to manipulate the on-chip fluid flow. By combining several micro-valves, more complex units like mixers, micro-pumps, multiplexers etc. can be built up, with thousands of units being accommodated on a single chip. In droplet-based biochips, the liquid is manipulated as discrete droplets on an electrode array.

Although biochips are becoming more complex everyday, Computer-Aided Design (CAD) tools for these chips are still in their infancy. Most CAD research has been focused on device-level physical modeling of components. Designers are using full-custom and bottom-up methodologies involving many manual steps to implement these chips. However, for both types of biochip, the synthesis process can be similar to that of designing microelectronics. This talk will illustrate how techniques and methods for designing multi-core microelectronic platforms can be used to solve synthesis and optimization problems of biochips. In particular, we will show how the high-level mapping process of multi-core microelectronic applications, can be used to map a biochemical application onto a given biochip architecture, by determining the resource allocation, binding, scheduling, placement and routing of the operations of the application.
08:00 — Registration
08:30 — Opening
Location: Convención
09:00 — Keynote Speech - 1
Location: Convención
Chair: Eugenio Villar
“Computing Platforms for the XXI Century” (Ian Phillips)
10:00 — Sessions
......................................................................................................  SPPI-I: Lean and Agile Processes
Location: Murcia
Chair: Rick Rabiser
Synthesizing a Comprehensive Framework for Lean Software Development
Henrik Jonsson, Stig Larsson and Sasikumar Punnekkat
Kanban in software development: A systematic literature review
Muhammad Ovais Ahmad, Jouni Markkula and Markku Oivo

................................................................................................  MOCS-I: Model-Driven Development I
Location: Granada
Chair: TBD
Model-to-Code transformation from Product-Line Architecture Models to AspectJ
Jessica Díaz, Jennifer Perez, Carlos Fernández Sánchez and Juan Garbajosa
Towards Component-based Domain Engineering
Asmaa Alayed, Kung-Kiu Lau, Petr Stepan and Cuong Tran

......................................................................................................  ESE-I: Model-Based Development
Location: Nixe P.
Chair: Etienne Borde
Framework for the design of firm Java real-time systems oriented to the generation of timing behaviour models
Patricia López Martínez, José M. Martínez Lanza, José M. Drake and Michael González Harbour
A Holistic (Component-based) Approach to AUTOSAR Designs
Kung-Kiu Lau, Petr Stepan, Cuong M. Tran, Sébastien Saudrais and Borjan Tchakaloff

Using Component-based Middleware to Design and Implement Data Distribution Service (DDS) Systems

Dennis Feiick and James Hill

11:00 — Coffee Break / Poster Session P1

11:30 — Sessions

........................................................................... SPPI-2: Improving Development Quality and Testing
Location: Murcia
Chair: Stefan Biffl

State-of-Practice in GUI-based System and Acceptance Testing: An Industrial Multiple-Case Study
Grischa Liebel, Emil Alégroth and Robert Feldt

Transformations between Various Composite and Visitor implementations in Java
Akram Ajouli, Julien Cohen and Jean-Claude Royer

TDDHQ: Achieving Higher Quality Testing in Test Driven Development
Adnan Causevic, Sasikumar Punnekkat and Daniel Sundmark

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Location: Granada
Chair: TBD

Managing the Coupled Evolution of Metamodels and Textual Concrete Syntax Specifications
Ludovico Iovino, Davide Di Ruscio and Alfonso Pierantonio

A Toolchain for Home Automation Controller Development
Peter Dalsgaard, Thibaut Le Guilly, Daniel Middelhede, Petur Olsen, Thomas Pedersen, Anders P. Ravn and Arne Skou

Towards Incremental Round-Trip Engineering Using Model Transformations
Thomas Buchmann and Bernhard Westfechtel

Img2UML: A System for Extracting UML Models from Images
Bilal Karasneh and Michel Chaudron

Wednesday, 4 September 2013
11:00 – Sessions

Location: Nixe P.

Chair: Patricia López Martínez

Early and Accurate Modeling of Streaming Embedded Applications
Richard Lee, Frederic Risacher and Samar Abdi

SEAL: a Domain-Specific Language for Novice Wireless Sensor Network Programmers
Atis Elsts, Jānis Judvaitis and Leo Selavo

Investigation of the influence of non-E/E safety measures for ASIL determination
Helmut Martin, Bernhard Winkler, Andrea Leitner, Alexander Thaler, Martin Cifrain and Daniel Watzenig

Software Module Real-Time Target: Improving Development of Embedded Control System by Including Simulink Generated Code into Existing Code
Øyvind Netland and Amund Skavhaug

13:00 — Lunch Break

14:30 — Keynote Speech - 2

Location: Convención

Chair: José Silva Matos

“Resilient Architectures for Energy-Efficiency” (Antonio González)

15:30 — Sessions

Location: Murcia

Chair: Fritz Stallinger

Variations on the Evidence-Based Timeline Retrospective Method A Comparison of Two Cases
Elizabeth Bjarnason, Anne Hess, Joerg Doerr and Björn Regnell

Objective Measurement of Safety in the Context of IEC 61508-3
Alois Mayr, Reinhold Ploesch and Matthias Saft

Risk-aware Migration of Legacy Data Structures
Matthias Book, Simon Grapenthin and Volker Gruhn

Feature-to-Code Traceability in a Collection of Product Variants Using Formal Concept Analysis and Information Retrieval
Hamzeh Eyal-Salman, Abdelhak Seriai and Christophe Dony

Wednesday, 4 September 2013
MOCS-3: Model Analysis and Interpretation

Location: Granada
Chair: TBD

Fast Evaluation of Power Consumption of Embedded Systems using DIPLODOCUS
Feriel Ben Abdallah and Ludovic Apvrille

Software Components Compatibility Verification Based on Static Byte-Code Analysis
Kamil Jezek, Premek Brada, Lukas Holy and Antonin Slezacek.

Towards Translational Execution of Action Language for Foundational UML
Federico Ciccozzi, Antonio Cicchetti and Mikael Sjödin

ESE-3: Requirements Engineering

Location: Nixe P.
Chair: TBD

Model-Driven Requirements Engineering for Embedded Systems Development
Grzegorz Loniewski, Etienne Borde, Dominique Blouin and Emilio Insfran

Embedded Systems Design Flows: Integrating Requirements Authoring and Design Tools
Ronald Wolvers and Tiberiu Seceleanu

A Context-based Information Retrieval Technique for Recovering Use-Case-to-Source-Code Trace Links in Embedded Software Systems
Jiale Zhou, Yue Lu and Kristina Lundqvist

17:00 — 17:30 Coffee Break / Poster Session P2

Welcome Reception
SEAA Sessions

Thursday, 5 September 2013

08:00 — Registration

08:30 — Keynote Speech - 3
Location: Convención
Chair: Onur Demirors
“Gummy Modules for Coping with Emergent Behaviour” (Mehmet Aksit)

09:30 — Sessions
Location: Murcia
Chair: TBD

Archetypical Approaches of Fast Software Development and Slow Embedded Projects
Ulrik Eklund and Jan Bosch

A Lean Approach to Estimate the Functional Size of Operating Applications
Filomena Ferrucci, Carmine Gravino and Guido Moretto

SM-1

09:30 — Sessions
Location: Granada
Chair: TBD

Microevolution of Pervasive Services
Mauro Caporuscio

Verifying Runtime Architectural Reconfiguration of Dynamically Adaptive Systems
Sihem Loukil, Slim Kallel and Mohamed Jmaiel

MOCS-4: Architecture Evolution

10:30 — 11:00 Coffee Break / Poster Session P3

11:00 — 11:30 Coffee Break / Poster Session P3

ESE-4: Formal Methods
Location: Nixe P.
Chair: Jan Carlson

Trace-Guided Synthesis of Reactive Behavior Models of Programmable Logic Controllers
Roland Schatz and Herbert Praehofer

Validating EAST-ADL Timing Constraints using UPPAAL
Jagadish Suryadevara
**SEAA Sessions**

**SM-2: EsPreSSE: Estimation and Prediction in Software & Systems Engineering**

**Location:** Murcia

**Chair:** Stefan Biffl

- **RisCal - A Risk Estimation Tool for Software Engineering Purposes**
  
  Christian Haisjackl, Michael Felderer and Ruth Breu

- **Static Prediction of Loop Iteration Counts Using Machine Learning to Enable Hot Spot Optimizations**
  
  Dirk Tetzlaff and Sabine Glesner

- **Software Product Complexity Estimation Using Grey Measurement**
  
  Semra Yilmaz Tastekin, Murat Erten and Semih Bilgen

- **Accuracy of Contemporary Parametric Software Estimation Models: A Comparative Analysis**
  
  Derya Toka and Oktay Turetken

**SPPI-4: MesVAM: Measurement as a Strategy for Software Value Management**

**Location:** Granada

**Chair:** Cigdem Gencel

- **Supporting Software Decision Meetings: Heatmaps for Visualising Test and Code Measurements**
  
  Robert Feldt, Miroslaw Staron, Erika Hult and Thomas Liljegren

- **Experiences and Insights from Applying GQM+Strategies in a Systems Product Development Organization**
  
  Jürgen Münch, Fabian Fagerholm, Petri Kettunen, Max Pagels and Jari Partanen

- **Industrial Challenges with Quality Requirements in Safety Critical Software Systems**
  
  Ali Shahrokni and Robert Feldt

**CS-1: Cloud Software**

**Location:** Nixe P.

**Chair:** Ivan Porres

- **LiRCUP: Linear Regression based CPU Usage Prediction Algorithm for Live Migration of Virtual Machines in Data Centers**
  
  Fahimeh Farahnakian, Pasi Liljeberg and Juha Plosila

- **A Computation and Storage Trade-off Strategy for Cost-Efficient Video Transcoding in the Cloud**
  
  Fareed Ahmed Jokhio, Adnan Ashraf, Sebastien Lafond and Johan Liljed

- **A Model for Policy based Automation of Usage Accounting across Multiple Cloud Infrastructures**
  
  Joachim Goetze, Tino Fleuren, Bernd Reuther and Paul Mueller
13:00 — Lunch Break

14:30 — Keynote Speech - 4
Location: Convención
Chair: Oktay Turetken
“Inside International Standards: A Contributor’s Perspective” (Rory O’Connor)

15:30 — Sessions

SM-3
Location: Murcia
Chair: TBD

- Overestimation and Underestimation of Software Cost Models: Evaluation by Visualization
  Nikolaos Mittas and Lefteris Angelis
- Identify Implicit Architectural Dependencies using Measures of Source Code Change Waves
  Miroslaw Staron and Wilhelm Meding

MOCS-5: Architecture Modeling
Location: Granada
Chair: TBD

- Analysing Architecture Description Languages for Formal Analysis, Usability, and Realisability
  Mert Ozkaya and Christos Kloukinas. Are We There Yet?
- Variability and Dependency Modeling of Quality Attributes
  José Miguel Horcas Aguilera, Mónica Pinto Alarcón and Lidia Fuentes Fernández
- Modelling for Hardware and Software Partitioning based on Multiple Properties
  tGaetana Sapienza, Tiberiu Seceleanu and Ivica Crnkovic
CS-2: Scientific Workflows in the Cloud

Location: Nixe P.
Chair: Ivan Porres

Facilitating Scientific Workflow Configuration With Parameterized Workflow Skeletons
Tino Fleuren, Paul Müller and Joachim Götte

Bringing Scientific Workflows to Amazon SWF
Matthias Janetschek and Radu Prodan

16:30 — 17:00 Coffee Break / Poster Session P4

19:00
Social Event

p. 43
08:30 — Registration

09:00 — Keynote Speech - 5

Location: Convención
Chair: Francesco Leporati

“Biochips: The Integrated Circuit of Biology” (Jan Madsen)

10:00 — Sessions

SPPI-5: Reuse and Evolution Processes

Location: Murcia
Chair: Rick Rabiser

Customer-Specific Teams for Agile Software Evolution
Helena Holmström Olsson, Jan Bosch and Hiva Alahyari

Improving Reusability in Software Process Lines
Emmanuelle Rouillé, Benoît Combemale, Olivier Barais, David Touzet and Jean-Marc Jézéquel

A Framework for Innovation Management System Customization for Product Line-based Software Businesses
Fritz Stallinger and Robert Neumann

TET-DEC-1: Workshop Session on Teaching, Education and Training for Dependable Embedded and Cyberphysical Systems [ERCIM/ARTEMIS/EUROMICRO]

Location: Granada
Chair: Erwin Schoitsch

Efficient embedded systems education by adapting component based software development paradigm
Sasikumar Punnekkat

Reuse in Safety Critical Systems: Educational Use Case
Miren Illarramendi Rezabal, Xabier Elkorobarrutia Letona, Leire Etxeberria

11:00 — Coffee Break / Poster Session P5
11:30 — Sessions

Location: Murcia
Chair: TBD

Applying EVM in a Software Company: Benefits & Difficulties
   Pinar Efe and Onur Demirors

Estimating the Effort to Develop Screen Mockups
   Giuseppe Scanniello, Filippo Ricca, Marco Torchiano, Carmine Gravino and Gianna Reggio

Approximate COSMIC size to early estimate Web application development effort
   Lucia De Marco, Filomena Ferrucci and Carmine Gravino

-----------------------------------------------
TET-DEC-2 Workshop Session on Teaching, Education and Training for Dependable Embedded and Cyberphysical Systems [ERCIM/ARTEMIS/EUROMICRO]

Location: Granada
Chair: Amund Skavhaug

Teaching and Training Formal Methods for Safety Critical Systems
   Michael Lipaczewski, Frank Ortmeier

European perspectives on Teaching, Education and Training for Dependable Embedded and Cyberphysical Systems
   Erwin Schoitsch, Amund Skavhaug

13:00 — Lunch Break

14:30 — Sessions
WiP2: Work In Progress

Location: Nixe P.
Chair: Konrad Kloeckner

Analyzing the Effects of Confirmation Bias on Software Development Team Performance: A Field Study during a Hackathon
Gul Calikli, Ayse Bener, Farid Shirazi

Semantic Technologies to Accelerate Model-Driven Development
Andreas Grünwald, Dietmar Winkler, Estefania Serral, Stefan Biffl

A Semantic Directory for Content and Partner Discovery in Empirical Software Engineering Research
Stefan Biffl, Juergen Musil, Estefania Serral, Dietmar Winkler

A Cost-Benefit Analysis Model for Technical Debt Management Considering Uncertainty and Time
Carlos Fernández-Sánchez, Jessica Díaz, Juan Garbajosa, Jennifer Pérez

Workflows on Manycore Processors: A Prospect
Matthias Janetschek, Radu Prodan

Languages for Safety-Certification Related Properties
Clara Benac Earle, Elena Gómez-Martínez, Stefano Tonetta, Stefano Puri, Silvia Mazzini, Jean-Louis Gilbert, Olivier Hachet, Ramon Serna, Oliver, Cecilia Ekelin, Katiusca Zedda

Towards Predicatable Dynamic Linking for Safety-Critical Component-Based Systems
Nermin Kajtazovic, Christopher Preschern, Norbert Druml, Christian Kreiner

Atlantis Access — Proposal for an Urban Accessibility for People with Physical Disabilities from the Perspective of Smart City
Eraldo Guerra, V. Lopes, I. Gomez
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- Poster Session P1 @ Convención (pag. 39)
- Poster Session P3 @ Convención (pag. 40)
- Poster Session P5 @ Convención (pag. 41)
- Control Room 1
- Control Room 2
- Busses departure to “Santillana del Mar”
DSD/SEAA 2013 will take place in Hotel Santemar
Joaquín Costa, 28, 39005 Santander

The city airport, Santander-Parayas (SDR), is connected (on a daily basis) with the two most important Spanish airports: Madrid-Barajas (MAD) and Barcelona-El Prat (BCN), both of which are very well connected with a large number of European cities. In addition, Ryanair provides some direct, low-cost flights that connect Santander with several European airports. Santander can also be reached via Bilbao Airport (BIO), which is about 115 km from Santander (approx. 1 hour and 15 minutes drive).

The Hotel Santemar, located on the exquisite beach of “El Sardinero” in a privileged environment, combines tradition and modernism, experience and efficiency and is distinguished by the style of the North in all its splendor. The large capacity both in bedrooms and conference rooms, it is the largest hotel in the north of Spain, makes it the ideal place to hold any kind of Convención in Santander, meetings, exhibitions or any other type of event.
Conference Rooms
As program chairs of the 2013 edition of DSD, the EUROMICRO Conference on Digital System Design we want to welcome you and to wish you a fruitful participation.

Our first words go to the authors who, in surprisingly high numbers, provided us with a considerable volume of high quality material, making it difficult the task of selecting the submissions that could be taken in. We do hope that all authors, regardless of whether their work was selected for presentation or not, did benefit from the comments and the recommendations offered by the more than 200 expert reviewers that helped us in this process. We further hope that those selected to present their work at the Conference will make the most of this opportunity. We hope they obtain useful feedback for their work, and have plenty of chances to discuss new ideas and to enlarge their network of contacts.

Paper reviewing is an extremely important job, one that sometimes goes unnoticed, and we would like to thank and recognize the generous work of the reviewers who could find precious time in their busy lifes to assess, comment and score papers submitted to DSD. This is a contribution that is right at the heart of the organization of a successful event. We are honored to have a distinguished set of Program Committee members who are highly recognized actors in all fields of digital system design. They are the true pillars of the success of DSD and their continued effort, expertise and wisdom is needed to keep raising the high level of scientific recognition that we have achieved. Our thanks to all of them and to the additional reviewers that were invited to help in this fundamental task.

Close to two hundred papers were submitted to DSD 2013, from 45 countries. Less than 50% were selected for oral presentation: forty four in the main track, and fifty four in the conference special sessions. Additionally, thirty two papers were selected for poster presentation and seven were invited to integrate the special session dedicated to ongoing activity in European R&D projects in the DSD area. All selected papers were subject to a rigorous review process that averaged more than three reviews per paper, and were ranked and thresholded according to their scores, weighted by the reviewers confidence.

From this high quality input, our job was simply to build the best possible program. To achieve this goal we worked with Eugenio Villar and his people at the University of Cantabria, and with the organizers of SEAA, agreeing on a common layout and choosing a set of highly-qualified keynote speakers that will motivate and interest audiences from both conferences. We put together a program that tries to achieve coherence in the sessions themselves, and also in the way they relate with each other, in line with the themes and the keynote speeches chosen for each day of the Conference. We believe we ended up with a rich and exciting program, but you will be the judges!

A lot of people worked hard to make this a memorable event. It is up to you now to participate actively, to enjoy the Conference, and make the most of it. Welcome to Santander. Welcome to DSD 2013.

José Silva Matos Francesco Leporati
EUROMICRO DSD 2013 Program Chairs
DSD Sessions

Wednesday, 4 September 2013

08:00 — Registration
08:30 — Opening
Location: Convención
09:00 — Keynote Speech - I
Location: Convención
Chair: Eugenio Villar
“Computing Platforms for the XXI Century” (Ian Phillips)
10:00 — Sessions

DSD-1: Interconnect Design
Location: Convención
Chairs: Kris Kuchcinski, Lech Jozwiak
Transient Fault Tolerant QDI Interconnects Using Redundant Check Code
Guangda Zhang, Wei Song, Jim Garside, Javier Navaridas and Zhiying Wang
Global Interconnect and Control Synthesis in System Level Architectural Synthesis Framework
Shuo Li and Ahmed Hemani

DSD-2: SoC&NoC (1)
Location: Palma
Chairs: Nicolas Sklavos, Victor Goulart
Analysis and evaluation of Circuit Switched NoC and Packet Switched NoC
Shaoteng Liu, Axel Jantsch and Zhonghai Lu
Parallel deadlock detection and recovery for networks-on-chip dedicated to diffused computations
Pierre Bomel and Marc Sevaux

SS2-1: MSDA 1 - Multicore Systems: Design and Applications
Location: Valencia
Chairs: Julio Sahuquillo, Anca Molnos
Run-time slack distribution for real-time data-flow applications on embedded MPSoC
Pavel G. Zaykov, Georgi Kuzmanov, Anca Molnos and Kees Goossens
Interaction of NoC design and Coherence Protocol in 3D-stacked CMPs
Pablo Abad, Pablo Prieto, Lucia G. Menez, Adrian Colaso, Valentín Puente and Jose Angel Gregorio
11:00 — Coffee Break / Poster Session P1

11:30 — Sessions

DSD-3: Modelling and Verification

Location: Convención
Chairs: Victor Fernandez, Alice Tokarnia

A Static Analysis Approach for Verification of Synchronization Correctness of SystemC Designs
Mikhail Moiseev, Mikhail Glukhikh and Sergey Salishev

Calibration Error Bound Estimation in Performance Modeling
Vidya Parappurath, Jeroen Voeten and Kees Kotterink

pCache: An Observable L1 Data Cache Model for FPGA Prototyping of Embedded Systems
Parthasarathy Ravishankar and Samar Abdi

Generation of Structural VHDL Code with Library Components
Sergey Ostroumov, Leonidas Tsiopoulos, Juha Plosila and Kaisa Sere

SS4-1: FTDSD 1 - Fault Tolerance in Digital System Design

Location: Palma
Chairs: Zdenek Kotasek, Peter Raab

Digital Late-Transition Metastability Simulation Model
Thomas Polzer and Andreas Steininger

Concurrent Error Detection in Multipliers by Using Reduced Wordlength Multiplication and Logarithms
Alexander Uhl and Juergen Becker

Identifying NBTI-Critical Paths in Nanoscale Logic
Raimund Ubar, Fabian Vargas, Maksim Jenihihin, Jaan Raik, Sergei Kostin and Leticia Bolzani Poehls

Efficient Construction of Global Time in SoCs despite Arbitrary Faults
Matthias Függer, Markus Hofstätter, Christoph Lenzen and Ulrich Schmid

SS1: FDR - Flexible Digital Radio

Location: Valencia
Chairs: Dominique Noguet, Co-Chair TBD

Stopping-free dynamic configuration of a multi-ASIP turbo decoder
Vianney Lapotre, Purushotham Murugappa, Guy Gogniat, Amer Baghdadi, Michael Huebner and Jean-Philippe Diguet

A Flexible Radio Transmitter for TVWS based on FBMC
Vincent Berg, Jean-Baptiste Doré and Dominique Noguet
A joint communication and application simulator for NoC-based custom SoCs: LDPC and turbo codes parallel decoding case study

Carlo Condo, Amer Baghdadi and Guido Masera

A Testbed for Evaluating LTE in High-Speed Trains

José Rodríguez-Piñeiro, Jose A. García-Naya, Ángel Carro-Lagoa and Luis Castedo

13:00 — Lunch Break

14:30 — Keynote Speech - 2

Location: Convención
Chair: José Silva Matos

“Resilient Architectures for Energy-Efficiency” (Antonio González)

15:30 — Sessions

DSD-4: Reconfigurable Computing (1)
Location: Convención
Chairs: Ahmed Hemani, Lech Jozwiak

Efficient Implementations of Multi-pumped Multi-port Register Files in FPGAs
Hasan Erdem Yantır, Salih Bayar and Arda Yurdakul

Dynamic Noise Estimation Approach for X-ray Detectors on FPGAs
Florian Aschauer, Walter Stechele and Johannes Treis

A Fast and Autonomous HLS Methodology for Hardware Accelerator Generation Under Resource Constraints
Adrien Prost-Boucle, Olivier Muller and Frederic Rousseau

An Efficient Hardware Implementation of a SAT Problem Solver on FPGA
Teodor Ivan and El Mostapha Aboulhamid

SS4-2: FTSD 2 - Fault Tolerance in Digital System Design
Location: Palma
Chairs: Maksim Jenihhim, Thomas Polzer

Software Modification Aided Transient Error Tolerance for Embedded Systems
Rishad A Shafik, Gerard Rauwerda, Jordy Potman, Kim Sunesen, Dhiraj K Pradhan, Jimson Mathew, Ioannis Sourdis

Methodology for Fault Tolerant System Design Based on FPGA Into Limited Redundant Area
Lukas Miculka, Martin Straka and Zdenek Kotasek

Virtual TMR Schemes Combining Fault Tolerance and Self Repair
T. Koal, M. Ulbricht and H. T. Vierhaus
Data Flow Analysis of Software Executed by Unreliable Hardware

Peter Raab, Stanislav Racek, Stefan Kraemer and Juergen Mottok

SS9-1: EPDSD I - European Projects in Digital System Design

Location: Valencia

Chairs: Lech Jozwiak, Francesco Leporati

SMAC: Smart Systems Co-Design
Nicola Bombieri, Dimitrios Drogoudis, Giuliana Gangemi, Renaud Gillon, Enrico Macii, Massimo Poncino, Salvatore Rinaudo, Francesco Stefanni, Dimistrios Trachanis and Mark van Helvoort

MultiPARTES: Multicore virtualization for Mixed-criticality Systems
Salvador Trujillo, Alfons Crespo and Alejandro Alons

E2LP: A Unified Embedded Engineering Learning Platform
Miodrag Temerinac, Ivan Kastelan, Karolj Skala, Branka Medved Rogina, Leonhard Reindl, Florent Souvestre, Margarita Anastassova, Roman Szewczyk, Jan Piwinski, Jorge R. Lopez Benito, Enara Artetxe Gonzalez, Nikola Tesic, Vlado Sruk and Moshe Barak

The TERAFLUX Project: Exploiting the DataFlow Paradigm in Next Generation Teradevices

17:00 — Coffee Break / Poster Session P2

17:30 — Sessions

DSD-5: NoC Routing

Location: Convención

Chairs: Arda Yurdakul, Dominique Houzet

An Effective Routing Algorithm to Avoid Unnecessary Link Abandon in 2D Mesh NoCs
Changlin Chen and Sorin Cotofana

Router Designs for an Asynchronous Time-Division-Multiplexed Network-on-Chip
Evangelia Kasapaki, Jens Sparso, Rasmus Sorensen and Kees Goossens

Power and Variability Improvement of an Asynchronous Router using Stacking and Dual-Vth Approaches
Mohammad Mirzaei, Mahdi Mosaffa, Siamak Mohammadi and Jelena Trajkovic
DSD Sessions

SS6-1: AHSA 1 - Architectures and Hardware for Security Applications

Location: Palma

Chairs: Paris Kitsos, Jens-Peter Kaps

Emulation-Based Fault Effect Analysis for Resource Constrained, Secure, and Dependable Systems

Norbert Druml, Manuel Menghin, Daniel Kroisleitner, Christian Steger, Weiss Reinhold, Armin Krieg, Holger Bock and Josef Haid

Electromagnetic Analysis on RSA Algorithm Based on RNS

Guilherme Perin, Laurent Imbert, Lionel Torres and Philippe Maurine

Double-Edge Transformation for Optimized Power Analysis Suppression Countermeasures

Shohreh Sharif Mansouri and Elena Dubrova

SS9-2: EPDSD 2 - European Projects in Digital System Design

Location: Valencia

Chairs: Francesco Leporati, Lech Jozwiak

parMERASA — Multi-Core Execution of Parallelised Hard Real-Time Applications Supporting Analysability


EU FP7-288307 - PHARAON project Parallel and heterogeneous architecture for real-time applications


Coarse-grain Optimization and Code Generation for Embedded Multicore Systems

George Goulas, Christos Valouxis, Panayiotis Alefragis, Nikolaos S. Voros, Christos Gogos, Oliver Oey, Timo Stripf, Thomas Bruckschloegl, Juergen Becker, Ali El Moussawi, Maxime Naulet and Tomofumi Yuki

Welcome Reception
Thursday, 5 September 2013

08:00 — Registration
08:30 — Keynote Speech - 3
Location: Convención
Chair: Onur Demirors
“Gummy Modules for Coping with Emergent Behaviour” (Mehmet Aksit)

09:30 — Sessions
DSD-6: Optimization and performance
Location: Convención
Chairs: Ian Philips, Arda Yurdakul
Distributed Runtime Computation of Constraints for Multiple Inner Loops
Nasim Farahini, Ahmed Hemani and Kolin Paul
A Formal Model for Optimal Autonomous Task Hibernation in Constrained Embedded Systems
Carlo Brandolese, William Fornaciari and Luigi Rucco
Multiobjective Optimization of Cost, Performance and Thermal Reliability in 3DICs
Fatemeh Kashfi and Jeff Draper

DSD-7: Video
Location: Palma
Chairs: Pablo Sanchez, Amund Skavaugh
Scalable Video Coding Deblocking Filter FPGA and ASIC implementation using High-Level Synthesis Methodology
Pedro P. Carballo, Omar Espino, Romén Noris, Pedro Hernández-Fernández, Tomasz M. Szydzik and Antonio Nunez
Architecture Design and Efficiency Evaluation for the High-Throughput Interpolation in the HEVC Encoder
Grzegorz Pastuszak and Maciej Trochimiuk.
A novel Intra prediction architecture for the hardware HEVC encoder
Andrzej Abramowski and Grzegorz Pastuszak
**SS3-1: DTDS 1 - Dependability and Testing of Digital Systems**

**Location:** Valencia

**Chairs:** Hana Kubatova, Muhammad Aamir Khan

- Minimal Stimuli Generation in Simulation-based Verification
  - **Shuo Yang, Robert Wille, Daniel Grosse and Rolf Drechsler**

- Simulation and SAT Based ATPG for Compressed Test Generation
  - **Jiří Balcárek, Petr Fišer and Jan Schmidt**

- Industrial Application of IEEE P1687 for an Automotive Product
  - Martin Keim, Tom Waayers, Richard Morren, Friedrich Hapke and Rene Krenz-Baath

**11:00 — Coffee Break / Poster Session P3**

**11:30 — Sessions**

**DSD-8: SoC&NoC (2)**

**Location:** Convención

**Chairs:** Victor Goulart, Nicolas Sklavos

- An Energy-Efficient Reconfigurable NoC Architecture with RF-Interconnects
  - **Majed Valadbeigi, Farshad Safaei and Bahareh Pourshirazi**

- Monitoring-Aware Virtual Platform Prototype of Heterogeneous NoC-based Multicore SoCs
  - **Miltos Grammatikakis, Antonis Papagrigoiou, Polydoros Petrakis and George Kornaros**

- An adaptive output selection function based on a fuzzy rule base system for Network on Chip
  - **Giuseppe Ascia, Maurizio Palesi and Vincenzo Catania**

- Incorporating Energy and Throughput Awareness in Design Space Exploration and Run-time Mapping for Heterogeneous MPSoCs
  - **Pham Nam Khanh, Amit Kumar Singh, Akash Kumar and Khin Mi Mi Aung**

**DSD-9: Reconfigurable Computing (2)**

**Location:** Palma

**Chairs:** João C. Ferreira, José S. Matos

- Energy-Aware Fault-Tolerant CGRAs Addressing Application with Different Reliability Needs
  - **Syed Mohammad Asad Hassan Jafri, Stanislaw Pietrak, Kolin Paul, Ahmed Hemani, Juha Plosila and Hannu Tenhunen**

- FPGA based real-time data processing DAQ system for the Mercury Imaging X-ray Spectrometer
  - **Florian Aschauer, Walter Stechele and Johannes Treis**
Component-Level Datapath Merging in System-Level Design of Wireless Sensor Node Controllers for FPGA-based Implementations

Muhammad Adeel Pasha, Steven Derrien and Olivier Sentieys

Automatic Hard Block Inference on FPGAs

Adrian Willenbücher and Klaus Schneider

SS3-2: DTDS 2 - Dependability and Testing of Digital Systems

Location: Valencia

Chairs: Petr Fiser, Martin Keim

Predictive Analysis of Mission Critical Systems Dependability

Martin Danhel, Hana Kubatova and Radek Dobias

A Distributed BIST Scheme for NoC-based Memory Cores

Bibhas Ghoshal and Indranil Sengupta

The Essence of Reliability Estimation during Operational Life for Achieving High System Dependability

Muhammad Aamir Khan and Hans G. Kerkhoff

Cone of Influence Analysis at the Electronic System Level Using Machine Learning

Jannis Stoppe, Robert Wille and Rolf Drechsler

13:00 — Lunch Break

14:30 — Keynote Speech - 4

Location: Convención

Chair: Oktay Turetken

“Inside International Standards: A Contributor’s Perspective” (Rory O’Connor)

15:30 — Sessions

SS2-2: MSDA 2 - Multicore Systems: Design and Applications

Location: Convención

Chairs: Julio Sahuquillo, Anca Molnos

A Multithreaded Parallel Global Routing Method with Overlapped Routing Regions

Yasuhiro Shintani, Masato Inagi, Shinobu Nagayama and Shin’ichi Wakabayashi

Advanced Switching Mechanisms for Forthcoming On-chip Networks

Emilio Castillo, Cristóbal Camarero, Esteban Stafford, Fernando Vallejo, Jose Luis Bosque and Ramon Beivide
SS6-2: AHSA 2 - Architectures and Hardware for Security Applications

Location: Palma
Chairs: Jens-Peter Kaps, Paris Kitsos

- Laser-Induced Fault Simulation
  Feng Lu, Giorgio Di Natale, Marie-Lise Flottes and Bruno Rouzeyre

- FPGA design of an Open-Loop TRNG
  Florent Lozach, Molka Benromdhane, Tarik Graba and Jean-Luc Danger

SS7-1: MRES 1 - Management and Reconfiguration of Embedded Systems

Location: Valencia
Chairs: Pasi Liljeberg, Pablo Ituero

- An Ambient Temperature Variation Tolerance Scheme for an Ultra Low Power Shared-L1 Processor Cluster
  Daniele Bortolotti, Andrea Bartolini and Luca Benini

- A resource manager for dynamically reconfigurable FPGA-based embedded systems
  Teresa G. Cervero, Ana Gómez, Sebastian López, Roberto Sarmiento, Julio Dondo, Fernando Rincón and Juan Carlos López

16:30 — Coffee Break / Poster Session P4
17:00 — Sessions

DSD-10: Applications

Location: Convención
Chairs: Amund Skavaugh, Pablo Sanchez

- Wireless Multi-Channel Quasi-Digital Tactile Sensing Glove-Based System
  Paolo Motto Ros, Marco Crepaldi, Alberto Bonanno and Danilo Demarchi

- Low Complexity Background Subtraction for Wireless Vision Sensor Node
  Muhammad Imran, Naeem Ahmad, Khursheed Khursheed, Mattias O’Nils and Najeem Lawal

- A Low Power 15-Bit Decimator in 0.18um CMOS for Biomedical Applications
  Kristin Scholfield and Tom Chen
SS6-3: AHSA 3 - Architectures and Hardware for Security Applications

Location: Palma

Chairs: Francesco Leporati, Paris Kitsos

- FPGA PUF based on Programmable LUT Delays
  Bilal Habib, Kris Gaj and Jens-Peter Kaps

- A Security-Enhanced UHF RFID Tag Chip
  Johann Ertl, Thomas Plos, Martin Feldhofer, Norbert Felber and Luca Henzen

- A Faster Shift-register Alternative to Filter Generators
  Ming Liu, Shohreh Sharif Mansouri and Elena Dubrova

SS7-2: MRES 2 - Management and Reconfiguration of Embedded Systems

Location: Valencia

Chairs: Pasi Liljeberg, Pablo Ituero

- A scalable hardware implementation of a best-effort scheduler for multicore processors
  Daniel Gregorek, Christof Osewold and Alberto García-Ortiz

- A Low-Area Reference-Free Power Supply Sensor
  Carlos Benito, Pablo Ituero and Marisa López-Vallejo

- Scenario Patterns and Trace-based Temporal Verification of Reactive Embedded Systems
  Alice Tokarnia and Emerson Cruz

Social Event

p. 43
DSD Sessions

Friday, 6 September 2013

08:30 — Registration

09:00 — Keynote Speech - 5

Location: Convención
Chair: Francesco Leporati

“Biochips: The Integrated Circuit of Biology” (Jan Madsen)

10:00 — Sessions

DSD-11: Adaptive Communication Techniques

Location: Convención
Chairs: Dominique Noguet, Antonio Nuñez

Adaptive Equalizer Training For High-Speed Low-Power Communication Systems
Yuan Fang, Ling Chen, Ashok Jaiswal, Peter Gregorius and Klaus Hofmann

Adaptive Low-Power Synchronization Technique for Multiple Source-Synchronous Clocks in High-Speed Communication Systems
Ashok Jaiswal, Yuan Fang, Peter Gregorius and Klaus Hofmann

DSD-12: SoC&NoC (3)

Location: Palma
Chairs: Sebastian López, Julio Dondo

AUTO-GS: Self-optimization of NoC Traffic Through Hardware Managed Virtual Connections
Muhammad Aurang Zaib, Jan Heisswolf, Andreas Weichslgartner, Thomas Wild, Juergen Teich, Juergen Becker and Andreas Herkersdorf

Design Tradeoffs of Long Links in Hierarchical Tiled Networks-on-Chip
Ran Manevich, Leon Polishuk, Israel Cidon and Avinoam Kolodny

SS8-1: DCPS 1 - Design of Cyber-Physical Systems

Location: Valencia
Chairs: Davide Quaglia, Emad Ebeid

morphone.OS: context-awareness in everyday life
Alessandro Antonio Nacci, Matteo Mazzucchelli, Martina Maggio, Alessandra Bonetto, Donatella Sciuto and Marco Domenico Santambrogio

UML-based Modeling and Simulation of Environmental Effects in Networked Embedded Systems
Emad Ebeid, Franco Fummi, Davide Quaglia
DSD-13: SHES - System Hardware and Embedded Software

Location: Convención
Chairs: Alice Tokarnia, João C. Ferreira

- Instruction Selection and Scheduling for DSP Kernels on Custom Architectures
  Mehmet Ali Arslan and Krzysztof Kuchcinski

- Register Transfer Level Workflow for Application and Evaluation of Soft Error Mitigation Techniques
  Filipe José P. Alves De Sousa, Francis Anghinolfi and João Canas Ferreira

- RAPIDITAS: RAPId Design-space-exploration Incorporating Trace-based Analysis and Simulation
  Amit Kumar Singh, Anup Das and Akash Kumar

- Automatic Controller Detection for Large Scale RTL Designs
  Wei Song and Jim Garside

SS4-3: FTDSD 3 - Fault Tolerance in Digital System Design

Location: Palma
Chairs: Petr Fiser, Tobias Koal

- Error Correction of Transient Errors in a Sum-Bit Duplicated Adder by Error Detection
  Stefan Weidling, Egor Sogomonyan and Michael Goessel

- Self-Checking Carry Select Adder with Fault Localization
  Muhammad Ali Akbar and Jeong-A Lee

- Area-Time Efficient Self-Checking ALU based on Scalable Error Detection Coding
  Zahid Ali Siddiqui, Park Hui-Jong and Jeong-A Lee

SS5: EEES - Energy Efficient Embedded Systems

Location: Valencia
Chairs: Marc Geilen, Antonio Nuñez

- Effective Online Power Management with Adaptive Interplay of DVS and DPM for Embedded Real-time System
  Gang Chen, Kai Huang, Jia Huang, Christian Buckl and Alois Knoll

- Energy Consumption Modeling of H264/AVC Video Decoding for GPP and DSP
  Yahia Benmoussa, Jalil Boukhobza, Eric Senn and Djamel Benazzouz
Power and Thermal Fault Effect Exploration Framework for Reader / Smart Card Designs
Norbert Druml, Manuel Menghin, Tobias Rauter, Christian Steger, Weiss Reinhold, Christian Bachmann, Holger Bock and Josef Haid

PtNBridge - A Power-aware and trustworthy Near Field Communication Bridge to Embedded Systems
Manuel Menghin, Norbert Druml, Manuel Trebo Fioriello, Christian Steger, Reinhold Weiss, Holger Bock and Josef Haid

13:00 — Lunch Break
14:30 — Sessions

DSD-14: Digital System Design
Location: Palma
Chairs: Chair Jan Madsen, Antonio Nuñez

Master-Slave Control structure for massively parallel System on Chip
Hana Krichene, Mouna Baklouti, Jean-Luc Dekeyser, Philippe Marquet and Mohamed Abid

Improving Performance and Fabrication Metrics of Three-Dimensional ICs by Multiplexing Through-Silicon Vias
Mostafa Said Sayed Abdelrehim, Farhad Mehdipour and Mohammed Ragab

LiChEn: Automated Electrical Characterization of Asynchronous Standard Cell Libraries
Matheus T. Moreira, Carlos H. M. Oliveira, Ney L. V. Calazan and Luciano C. Ost

Runtime Online Links Voltage Scaling for Low Energy Networks on Chip
Andrea Mineo, Maurizio Palesi, Giuseppe Ascia and Vincenzo Catania

SS6-4: AHSA 4 - Architectures and Hardware for Security Applications
Location: Valencia
Chairs: Paris Kitsos, Francesco Leporati

Glitch Detection in Hardware Implementations on FPGAs using Delay Based Sampling Techniques
Rajesh Velegalati, Kinjal Shah and Jens-Peter Kaps

Evaluating the Hardware Performance of the Gentry-Halevi FHE Scheme
Yarkin Doroz, Erdinc Ozturk and Berk Sunar

PERMS: A Bit Permutation Instruction For Accelerating Software Cryptography
Souvik Kolay, Sagar Khurana, Anupam Sadhukhan, Chester Rebeiro and Debdeep Mukhopadhyay

A Scalable Multiplier for Arbitrary Large Numbers Supporting Homomorphic Encryption
Ghada Abozaid, Ahmed El-Mahdy and Yasutaka Wada
SS8-2: DCPS 2 - Design of Cyber-Physical Systems

**Location:** Murcia

**Chairs:** Emad Ebeid, Davide Quaglia

- *Fast Multiprocessor Scheduling with Fixed Task Binding of Large Scale Industrial Cyber Physical Systems*
  Shreya Adyanthaya, Marc Geilen, Twan Basten, Ramon Schiffelers, Bart Theelen and Jeroen Voeten

- *Towards a Modelling and Design Framework for Mixed-Criticality SoCs and Systems-of-Systems*
  Fernando Herrera, Seyed Hosein Attarzadeh Niaki and Ingo Sander

- *Passivity-Based Control over Differentiated-Services Packet Networks*
  Giovanni Lorenzi, Davide Quaglia, Riccardo Muradore and Paolo Fiorini

- *A Physical-aware Abstraction Flow for Efficient Design-space Exploration of a Wireless Body Area Network Application*
  Marco Crepaldi, John Buckley, Davide Quaglia, Brendan O’Flynn and Danilo Demarchi

**WiP 1: Work In Progress**

**Location:** Granada

**Chair:** Erwin Grosspietsch

- *A Fast Memory Access Circuit Synthesis*
  Takashi Kambe, Shuji Tsukiyama

- *A Clustered Globally Asynchronous Locally Synchronous Network-on-Chip Communication Architecture*
  Kazem Cheshmi, Siamak Mohammadi, Djamshid Tavangarian, Jelena Trajkovic, Daniel Versick

- *QR Decomposition via Householder Reflectors on FPGA Technology*
  Alessandro Barberis, Francesco Leporati

- *New SEU Modeling by Architecture Analysis*
  Jan Pospisil, Jan Schmidt, Petr Fiser

- *Different Implementations for Destressing k out of n:G Systems*
  Markus Ulbricht, Heinrich Theodor Vierhaus

16:00 — 16:30 Coffee Break
**DSD Poster Sessions**

Wednesday, 4 September 2013

**11:00 — 11:30 Poster Session P1**

**Olympic: a Hierarchical All-optical Photonic Network for Low-power Chip Multiprocessors**
Sandro Bartolini, Luca Lusnig and Enrico Martinelli.

**Non-Intrusive NoC DFS for Soft Real-Time Multimedia Applications**
Miltos Grammatikakis, Antonis Papagrigoriou, Polydoros Petrakis and George Kornaros

**Early performance evaluation of Multi-OS embedded platforms using native simulation**
Rodrigo Fernández, Hector Posadas and Eugenio Villar

**Impact of 3D IC on NoC Topologies: A Wire Delay Consideration**
Mohamad Hairol Jabbar, Dominique Houzet and Omar Hammami

**High Performance Bitwise OR Based Submesh Allocation for 2D Mesh-connected CMPs**
Luka Daoud and Victor Goulart

**A General Framework for Average-Case Performance Analysis of Shared Resources**
Sahar Foroutan, Benny Akesson, Kees Goossens and Frederic Petrot

**17:00 — 17:30 Poster Session P2**

**Novel dynamic gate topology for superpipelines in DSM**
Juan Nuñez, María José Avedillo and José María Quintana

**Comparison of FPGA and ASIC Implementation of a Linear Congruence Solver**
Jiri Bucek, Pavel Kubalik, Robert Lorenz and Tomas Zahradnicky

**VLSI Architecture for Low-Complexity Motion Estimation in H.264/MVC Multiview Video Coding**
Ashfaq Ahmed, Muhammad Usman Shahid, Maurizio Martina, Enrico Magli and Guido Masera

**A Flexible and Compact Regular Expression Matching Engine Using Partial Reconfiguration for FPGA**
Yoichi Wakaba, Shinobu Nagayama, Shin’ichi Wakabayashi and Masato Inagi

**An Efficient Router Architecture and its FPGA Prototyping to support Junction Based Routing in NoC Platforms**
M. Awais Aslam, Shashi Kumar and Rickard Holsmark

**An Efficient FPGA-Based Architecture of Skein for Simple Hashing and MAC Function**
Filippos Pirpilidis and Paris Kitsos

**Implementing Modular FFTs in FPGAs — A Basic Block for Lattice-Based Cryptography**
Tamás Györfi, Octavian Creț and Zalán Borsos
11:00 — 11:30 Poster Session P3

**Execution Time and Code Size Optimization using Multidimensional Retiming and Loop Striping**  
Yaroub Elloumi, Mohamed Akil and Mohamed Hedi Bedoui

**UML/MARTE Methodology For Automatic SystemC Code Generation of OPENMAX Multimedia Applications**  
Pablo Peñil, Pablo Sanchez, David de La Fuente, Jesus Barba and Juan Carlos Lopez

**Efficient Instruction-set Architecture Exploration for Application Specific Processors**  
Roel Jordans, Rosilde Corvino, Lech Jozwiak and Henk Corporaal

**Delay Fault Coverage Increasing in Digital Circuits**  
Miroslav Siebert and Elena Gramatova

**Account for radiation effects in signal integrity analysis of PCB digital systems**  
Konstantin Petrosyants and Igor Kharitonov

**Voltage spikes on the substrate to obtain timing faults**  
Karim Tobich, Philippe Maurine, Pierre-Yvan Liardet, Mathieu Lisart and Thomas Ordas

16:30 — 17:00 Poster Session P4

**Designing DPA Resistant Circuits Using BDD Architecture and Bottom Pre-charge Logic**  
Partha De, Kunal Banerjee, Chittaranjan Mandal and Debdeep Mukhopadhyay

**Differential Power Analysis under Constrained Budget: Low Cost Education of Hackers**  
Filip Štěpánek, Jiří Buček and Martin Novotný

**Compact FPGA-based hardware architectures for GF($2^m$) multipliers**  
Miguel Morales-Sandoval and Arturo Díaz-Pérez

**MISRs for Fast Authentication of Long Messages**  
Rajendra Katti and Rucha Sule

**A Novel Authenticated Encryption Algorithm for RFID systems**  
Zahra Jeddi, Esmaeil Amini and Magdy Bayoumi

**Hardware Trojan Protection for Third Party IPs on FPGA**  
Amr Al-Anwar, Yousra Alkabani, M. Watheq El-Kharashi and Hassan Bedour

**Development flow for FPGA-based scalable reconfigurable systems**  
Julián Caba, Julio Daniel Dondo, Fernando Rincón, Jesus Barba and Juan Carlos López
Friday, 6 September 2013

11:00 — 11:30 Poster Session P5

Memristor-based (ReRAM) Data Memory Architecture in ASIP Design
Mathias Hartmann, Praveen Raghavan, Liesbet Van Der Perre, Prashant Agrawal and Wim Dehaene

Architecture and Implementation of a Data Compression System at Switch-Level in ATA-over-Ethernet Storage Networks
Angela Souto-Vieites and Roberto Osorio

Capacitive sensors matrix for interface pressure measurement in clinical, ergonomic and automotive environments
Elisa Marenzi, Gian Mario Bertolotti, Francesco Leporati and Giovanni Danese

A Novel Portable Surface Plasmon Resonance Based Imaging Instrument for On-Site Multi-Analyte Detection
Lab On Chip: Portable Optical Device for On-Site Multi-Parametric Analysis
Sara Rampazzi, Giovanni Danese, Lucia Fornasari, Francesco Leporati, Franco Marabelli, Nelson Nazzicari and Andrea Valsesia

Dataflow-based Multi-ASIP Platform Approach for Digital Control Applications
Raymond Frijns, Twan Kamp, Sander Stuijk, Jeroen Voeten, Marcel Bontekoe, John Gemei and Henk Corporaal

pyHybridAnalysis: a Package for epsilon-Semantics Analysis of Hybrid Systems
Alberto Casagrande and Tommaso Dreossi
On Wednesday, 4th of September, the City Mayor will welcome the conference participants to the city of Santander. The Reception will take place at the City Hall starting at 20h. The building is located downtown in the City Hall Square. The place is reachable in 30 min. by busses number 1, 2 or 7 from the ‘Plaza de Italia’, the square down the street from the Hotel Santemar.
The social event of the conference will take place on Thursday, 5th of September. The busses will be ready in front of the Santemar Hotel from 18h30m. Do not forget your invitation ticket to board the bus. They will bring the registered participants to the medieval city of Santillana del Mar. Participants will visit the town and the Romanic collegiate church. The dinner will take place in the ‘Parador Gil Blas’ located behind the main square of the town. The busses will bring the participants back to the hotel at 23h